UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,158	04/09/2004	Vamsi Boppana	162.8030USU	1180

7590 11/20/2006

Paul D. Greeley, Esq.
Ohlandt, Greeley, Ruggiero & Perle, L.L.P.
10th Floor
One Landmark Square
Stamford, CT 06901-2682

EXAMINER	
PARIHAR, SUCHIN	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,158	BOPPANA ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-26 and 28-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 12-26 and 28-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This FINAL office action is response to the amendment filed on 8/15/2006. Claims 1, 3-8, 10, 12-13, 15, 17, 19-24, 26, 28-29 and 31 are currently amended. Claims 11 and 27 are canceled. Claims 1-10, 12-26 and 28-32 are pending in this application.

Applicant's arguments, filed 8/15/2006, have been fully considered and are persuasive. However, upon further consideration, a new ground(s) of rejection is made. in view of the amendment and search update.

PD

Upon further consideration, the allowability of claims 5, 10, 21 and 26 has been withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 10 and 26 are rejected under 35 U.S.C. 112, second paragraph**, as being incomplete for omitting essential structural/functional cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections or functional steps. See MPEP § 2172.01. The omitted structural/functional cooperative relationships are: the relationship between "a diffusion region width, w, is estimated as Spp/2" and "a net associated with said diffusion region" is missing. It is not clear how "a net" is related to an estimation that results in Spp/2, i.e. what is the relationship between the estimation and the net?

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. **Claims 1-10, 12-26 and 28-32 are rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter.

6. With respect to claims 1 and 17, these claims are non-statutory because they fail to provide a useful, concrete, and tangible result. Specifically, the "estimating a value" and "obtain an estimated value of a parasitic" only provide abstract numbers as a result of the claim steps. Abstract numbers [values] do not provide a useful, concrete and tangible result within the claim language of claims 1 and 17.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 1-3, 6-8, 16-18, 22-24 and 32 are rejected under 35 U.S.C. 102(b)** as being anticipated by Ray et al (6,643,832).

9. With respect to claims 1 and 17, Ray teaches an automated computer-implemented method (i.e. computer aided design tool, Col 1, lines 45-47) and a medium including computer readable program instructions (see Fig 4, computer readable program instructions) comprising:

receiving a pre-layout representation (generating netlist, see Fig 1, 114) of a standard cell (HDL specification is synthesized into standard cells, Col 1, lines 29-32);

applying a transformation to said pre-layout representation (i.e. optimize netlist, see Fig 1, 116) to obtain an estimated value of a parasitic (estimating delays of cells in a netlist, Col 2, lines 54-56) of said standard cell (cells, i.e. standard cells, Col 2, lines 54-56); and

estimating (i.e. generating timing data) a value (whether a timing violation occurs at a particular cell, Col 4, lines 60-65) for a characteristic (i.e. timing analysis, Col 4, lines 60-65) of said standard cell (at each cell, Col 4, lines 60-61), based on said estimated value of said parasitic (i.e. delay estimation model, Col 5, lines 55-57).

10. With respect to claims 2 and 18 Ray teaches all the elements of claims 1 and 17, from which the claims depend respectively. Ray teaches: wherein said pre-layout representation is selected from the group consisting of a: spice netlist (i.e. netlist generated from a schematic diagram, Col 1, lines 45-48), a BDD-based transistor structure representation, and a pre-layout structural representation (interconnection between cells and logic structure, Col 4, lines 17-25).

11. With respect to claim 3, Ray teaches all the elements of claim 1, from which the claim depends. Ray teaches: wherein said estimating (i.e. estimating delays of logic gates in a netlist, Col 1, lines 20-25) is further based on a representative set of laid out cells (placing the selected cells at particular locations, Col 1, lines 49-52) for a particular technology and cell architecture (i.e. particular technology library, Col 1, lines 20-25).

12. With respect to claims 6 and 22, Ray teaches all the elements of claims 1 and 17, from which the claims depend respectively. Ray teaches: wherein said

characteristic is a parasitic-dependent standard cell characteristic (each cell has an associated cell definition having timing characteristics, Col 3, lines 50-54).

13. With respect to claims 7 and 23, Ray teaches all the elements of claims 1 and 17, from which the claims depend respectively. Ray teaches: wherein said characteristic is selected from the group consisting of: timing (i.e. optimization provides delay estimates for each structure using timing-based tree models, Col 4, lines 38-45), power, input capacitance (i.e. estimated capacitances at gate model's inputs), and noise.

14. With respect to claims 8 and 24, Ray teaches all the elements of claims 1 and 17, from which the claims depend respectively. Ray teaches: wherein said transformation is selected from the group consisting of: transistor folding, diffusion area and perimeter assigning (the cells of an optimized [i.e. transformed] netlist are placed by arranging the cells in particular locations [i.e. area/perimeter assigning] to form a layout pattern [i.e. transformation] for the integrated circuit, Col 4, lines 50-55) of transistors of said standard cell, and adding wiring capacitances to said pre-layout representation.

15. With respect to claim 16 and 32, Ray teaches all the elements of claims 1 and 17, from which the claims depend respectively. Ray teaches: wherein said characteristic is selected from the group consisting of: a cell footprint and a pin placement of said cell (i.e. delay for a specific output pin of the gate, Col 2, lines 45-50).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. **Claims 4, 5, 20 and 21 rejected under 35 U.S.C. 103(a)** as being unpatentable over Ray et al. (6,643,832) in view of Sato et al. (6,009,248).

18. With respect to claims 4, 5, 20 and 21, Ray fails to teach: wherein said estimating is accurate to within about 1.5 percent, and is accurate to within 5 percent of a post-layout value of said characteristic for said standard cell.

However, Sato teaches: wherein said estimating is accurate to within about 1.5 percent (i.e. enables optimization of about 15 to 20 percent, see Sato, Col 16, lines 12-17), and is accurate to within 5 percent (i.e. enables optimization of about 15 to 20 percent, see Sato, Col 16, lines 12-17) of a post-layout value of said characteristic for said standard cell (i.e. delay between a pre-layout delay and a post-layout delay is small, estimation of a delay value by the optimization is accurate, Col 16, lines 12-17).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Sato into the invention of Ray for at least the following reason: Sato improves the delay estimation and optimization method of Ray by providing an optimization system which conducts appropriate optimization to avoid iteration of optimization, thereby reducing required time of optimization (see Sato, Col 5, lines 36-42).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. **Claims 9, 15, 25 and 31 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Ray et al. (6,643,832) in view of McGuiness et al. (US PG Pub 2004/0078768).

21. With respect to claims 9 and 25, Ray fails to teach: wherein said transistor folding transformation is performed prior to said diffusion area and perimeter assigning of transistors of said standard cell transformation, and adding wiring capacitances to said pre-layout representation.

However, McGuiness teaches: wherein said transistor folding transformation (i.e. construct selected fold solution, see Fig 2) is performed prior to said diffusion area and perimeter assigning of transistors (see Fig 2, folding occurs at 35, which occurs prior to transistor placement 36 and Height and Width constraints 46 and 48 [proper assigning of height and width perimeter values as not to violate their respective constraints]) of said standard cell transformation, and adding wiring capacitances (according to claim 8 and 24, this may or may not take place) to said pre-layout representation.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate McGuiness into the invention of Ray for at least the following reasons: McGuiness improves the invention of Ray by providing a method of folding transistor cells which results in a reduction of cell height. It is well known in the art that a reduction in cell height helps prevent transistor cells from violating height and width constraints when the cells are placed and routed in a layout. Since Ray provides a step

wherein placement and routing is performed (see Fig 1, step 118), the transistor folding feature of McGuiness would improve the placement and routing step of Ray by providing a method of manipulating cell perimeter to allow for easier placement and routability. McGuiness also suggests that such transistor folding would be performed prior to any diffusion area and perimeter-assigning step, since the folding itself modifies the perimeter of the cells and would thus change diffusion area and perimeter assigning requirements.

22. With respect to claims 15 and 31, Ray teaches all the elements of claims 1 and 17, from which the claims depend respectively. Ray teaches: adding wiring capacitances to said pre-layout representation (large buffer trees [which have an associated capacitance] are often inserted into a netlist [pre-layout representation, see Fig 1, 114], Col 4, lines 23-30).

Ray fails to teach: diffusion area and perimeter assigning.

However, McGuiness teaches: diffusion area and perimeter assigning (see Fig 2, Height and Width constraints 46 and 48 [proper assigning of height and width perimeter values to satisfy constraints]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate McGuiness into the invention of Ray for at least the following reasons: McGuiness improves the invention of Ray by providing a method involving a reduction of cell height. It is well known in the art that a reduction in cell height helps prevent transistor cells from violating height and width constraints [i.e. perimeter dimensions] when the cells are placed and routed in a layout. Since Ray provides a

step wherein placement and routing is performed (see Fig 1, step 118), the height and width constraint checking of McGuiness would improve the placement and routing step of Ray by providing a method of manipulating cell perimeter to allow for easier placement and routability.

Allowable Subject Matter

23. Claims 12-14 and 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 12 and 28, the prior art made of record fails to teach: wherein said pre-layout representation is a pre-layout netlist and said transformation comprises adding a wiring capacitance to each net in said pre-layout netlist and a capacitance C(n) of a net is estimated as: (see equation of Claims 12 and 28)

Wherein α, β, and γ are constants, TDS(n) is a set of transistors whose drain or source is connected to a net n, TG(n) is a set of transistors whose gate is connected to said net n, MTS(t) is a maximal transistor series that includes a transistor t, and MTS(t) is a number of transistors in MTS(t).

Response to Arguments

25. Applicant's arguments, filed 8/15/2006, have been fully considered and are persuasive. Upon further consideration, a new ground(s) of rejection is made as described above.

26. Upon further consideration, the allowability of claims 5, 10, 21 and 26 has been withdrawn.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PAUL DINH
PRIMARY EXAMINER

Suchin Parihar
Examiner
AU 2825